Session 21 Overview

Advanced Clocking, Logic and Signaling Techniques

Chair: Thucydides Xanthopoulos, Cavium Networks, Marlboro, MA

Associate Chair: Sohichi Miyata, SHARP, Osaka, Japan

Clock generation and distribution has traditionally been an area of circuit innovation due to its impact on overall chip performance and cost. In the first half of the session, a series of clocking techniques are presented that address issues such as process independence, power dissipation, low jitter, low skew, and duty-cycle correctness.

Clock-powered logic families have generated interest in the past due to their potential for low power dissipation through adiabatic charge recycling. Clock frequencies in the 100s of MHz though dictated the use of external inductive clock generators. Process and frequency scaling has enabled faster logic and the potential of fully integrating resonant clock generators on chip. In papers in the second half of this session, clock-powered logic families in the 1 to 3GHz range are presented that use integrated LC and transmission-line-based oscillators.

Process and frequency scaling has made wire-inductance modeling a necessary part of the design process. In papers in this session, the exploitation of wire inductance for clock distribution and signal transmission is demonstrated.

Integrated PLLs have been traditionally used for digital clock generation. In Paper 21.1, an alternative method of low-frequency clock synthesis, using a free-running oscillator and digital processing logic, is presented. Controlled-frequency slew rate and spread-spectrum clocking are easily implemented with this technique.

Distributing clocks in large microprocessor chips has always been a challenge. In Paper 21.2, the clock generation and distribution of a dual-core Xeon™ processor are discussed. Multiple clock-domain management is also discussed.

Wire inductance presents multiple issues to the clock designer due to complex modeling, increased wire transit time and signal reflections. In Paper 21.3, a non-traditional clock-tree design is proposed that exploits transmission-line reflection effects for duty-cycle correction and PVT insensitivity of the overall insertion delay.

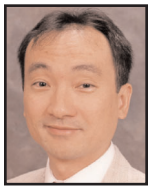
Wireless on-chip clock distribution can be a low-power low-skew alternative to traditional techniques. In Paper 21.4 a wireless receiver structure that converts an 18GHz RF clock signal to a GHz-range digital clock is discussed; it can be used in this context.

In Papers 21.5 and 21.6, multi-GHz clock-powered logic families that can use a fully integrated resonant clock generator (LC or transmission-line based) are presented. Substantial energy savings are being demonstrated.

Finally, in Paper 21.7 an on-chip interconnect methodology using a negative impedance converter adapted from analog long-distance telephony is presented. The impedance converter provides loss compensation while adding minimal latency to the signal path.

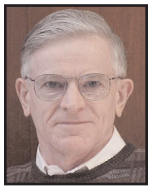
21.1 Free-Running Ring Frequency Synthesizer **1:30 PM**
D. Allen, TimeLab, Andover, MA

A digital processor uses a single free-running ring oscillator to synthesize multiple clocks without analog circuits or feedback loops. Fabricated in 0.18µm technology, the 4mm^2 die integrates 6 independent spread-spectrum synthesizers with <0.1ps period resolution. The synthesizers operate from 3 to 400MHz with a jitter <85ps, meeting PCIe clock-jitter requirements.



21.2 Clock Generation and Distribution of a Dual-Core Xeon™ Processor with 16MB L3 Cache **2:00 PM**
S. Tam, Intel, Santa Clara, CA

The clock generation and hybrid clock distribution for a dual-core Xeon™ processor with 16MB L3 cache are designed for <11ps global clock skew in a 435mm^2 die. The cache and control sections contain 2 primary clock domains and 11 clock spines. A pipelined de-skew logic tolerant to inter-domain clock uncertainties manages the core and cache/control data communication.



21.3 A 5GHz Duty-Cycle Correcting Clock Distribution Network for the POWER6 Microprocessor **2:30 PM**
M. Thomson, IBM, Yorktown Heights, NY

Microprocessor global clock distribution networks use long buffered wires where reflections can be significant. Using accurate transmission-line models and optimization, these reflection effects can be exploited to improve clock-distribution characteristics. The clock distribution network of the POWER6 microprocessor is designed to run at frequencies exceeding 5GHz using only inverters and transmission lines and is capable of on-the-fly duty-cycle correction.

21.4 A Receiver with Start-up Initialization and Programmable Delays for Wireless Clock Distribution **3:15 PM**
X. Guo, University of Florida, Gainesville, FL

A receiver for wireless clock distribution runs at 2.25GHz with 5ps$_{pp}$ jitter. The clock is distributed as a sine wave at 8 times the actual clock frequency to mitigate dispersion. The receiver includes an initialization circuit and a frequency divider with 16 quantized programmable delays for skew reduction.

21.5 A 1.1GHz Charge-Recovery Logic **3:45 PM**
V. Sathe, University of Michigan, Ann Arbor, MI

A GHz-class dynamic charge-recovery logic is implemented with an on-chip clock generator and integrated inductor in a 0.13µm CMOS process. The chip operation is verified at clock frequencies up to 1.3GHz. At its natural frequency, the design recovers 60% of total circuit energy every cycle.

21.6 A 3.5 GHz Rotary-Traveling-Wave-Oscillator Clocked Dynamic Logic Family in 0.25µm CMOS **4:15 PM**
C. Ziesler, Multigig, Scotts Valley, CA

Initial silicon results for a 3.5GHz dynamic logic family in 0.25µm SOI are presented. The chip is clocked with a rotary-traveling-wave oscillator, demonstrating per-gate dissipation of 100fJ per operation.

21.7 Distributed Loss Compensation for Low-latency On-chip Interconnects **4:45 PM**
A. Jose, Columbia University, New York, NY

The use of distributed loss compensation for on-chip interconnects is discussed. Results are presented for a 14mm 3Gb/s on-chip link in 0.18µm CMOS with a measured latency of 12.1ps/mm and an energy dissipation of 2pJ/b with a BER<10^{-14}. A 3× improvement in power consumption and a 1.5× improvement in latency over an optimally-repeated RC line is demonstrated.